IN THE SPECIFICATION

Please amend the Specification as follows:

On page 1, line 10:

The present invention relates generally to systems for processing routing and filtering information ~~FOR~~ for each packet received at a router node of a data transmission network, and in particular to an interleaved processing system based upon a tree lookup structure in a network router.

On page 8, line 1:

The right side of tree **100** starting from **A** and proceeding to node **C**, etc. represents a tree search including some binary elements and other more complex elements. For example, node **K** includes four branches that are selectable based on a two-bit analysis, and node **G** ~~which has~~ having two branches that are selectable based on a ~~comparison done on several long binary patterns (5 bits in the example)~~ five-bit analysis.

On page 9, line 16:

Bank[[s]] A **20** and Bank B **22** contain respectively the instructions associated with each node in a given tree. Activation signal carried from task scheduler **18** on activation lines **24** and **26** are utilized for loading an instruction from external memory **12** to one of banks **20** or **22** via external bus **14**. Activation signals on activation lines **24** and **26** also activate the transfer of an instruction from the other bank (the bank not being loaded from external memory **12**) to task processor **16** via an internal bus **28** for processing the instruction. At any given time, a bank has only one of the above access valid signals carried on bus **28** while the other bank has access to bus **14**. This bus connection is inverted at each edge of the thread clock allowing the process of an instruction on one tree while an instruction of the other tree is loaded into its corresponding bank. In a preferred embodiment of the present invention, one of ~~banks~~ Bank A **20** or Bank B **22** is associated with a source address tree while the other bank is associated with a destination address tree in an address lookup mechanism.

On page 14, line 28:

Turning now to **Fig. 5**, there is illustrated a representative format of ~~an~~ a lookup instruction utilized in the interleaved packet processing system of the present invention. As shown in **Fig. 5**, each lookup instruction contains three main fields. The first of these fields is an instruction field **72** that includes the instruction ~~itself that is~~ to be executed by the task processor. The second field in a comparison field, represented in the depicted embodiment as one or more of multiple comparison fields **74a-74n**, which contains the pattern previously stored within the external memory (in a table, for example) to compare with the **A** or **B** pattern that correspond to a source and destination address bit pattern at the current point of the address processing analysis. Finally, the lookup instruction includes a next address field, represented in the depicted embodiment as one or more of multiple next address fields **76a-76n**, that contains the addresses for the possible next instructions.

On page 15, line 10:

The instruction field ~~itself~~ **72** is generally defined in a single word. ~~The~~ As shown in the depicted embodiment, the contents of the instruction field ~~define~~ **72** include a MODE field specifying the mode of analysis to perform such as one bit, two bits or three bits full comparison resulting in two, four, or eight branches, or, whether a multi-bit pattern comparison should be performed using further comparison fields. The contents of instruction field ~~contents~~ also include a NBR OF COMP field[[s]] defining the number of elements (bits) within the comparison field, and the number of bits in the next address field that defines the size of the instruction and informs the processor of whether or not an instruction is fully loaded.

On page 15, line 22:

In full comparison mode, additional fields **76a-76n** are defined that identify the next address to use for each output case that can be a direct value or an indexed value. There is one such sub-field for each possible branch. **Fig. 5** illustrates a case ~~in which~~ having 4 branches corresponding to a two bits full comparison: branches 00 (B1 IX), 01 B2 IX), 10 (B3 IX) and 11 (B4 IX).

On page 15, line 29:

The index (IX) for each of the branch sub-fields B1 IX, B2 IX, B3 IX, and B4 IX is a 2-bit field that indicates the actual address value based on the address given as a base address. A value of 00 for IX indicates that the address is the address of the indicated next add field, while 01 instructs to increment by one the indicated next add field. An IX value of 10 instructs to increment by 2, and 11 to increment by 3. A single next add field allows for pointing onto up to 4 different instruction elements in memory thus reducing the size of the instruction itself.

On page 16, line 6:

The comparison field stores, ~~if any~~ in a COMPARISON PATTERN sub-field, the pattern(s) to compare to the bits starting at the current position in the A or B pattern field. For each pattern, a NB BITS sub-field indicates the length of the pattern ~~(Nbbits)~~, a possible mask (~~Pattern Mask~~ PATTERN MASK), the next address sub field (direct or indexed) to use or next comparison to perform ~~when match~~ depending on whether or not a match is found (FIELD IF K0, FIELD IF 0K). The index method is the same as what is defined in the instruction field. It should be noted that, when the link is performed on another comparison field, the index field (IX) is irrelevant.

The Abstract on page 22, line 1:

INTERLEAVED PROCESSING SYSTEM FOR PROCESSING FRAMES WITHIN A NETWORK ROUTER

ABSTRACT OF THE DISCLOSURE

~~**INTERLEAVED PROCESSING SYSTEM FOR PROCESSING FRAMES WITHIN A NETWORK ROUTER**~~

A system and method for performing interleaved packet processing ~~in a network router~~. A packet ~~to be routed~~ includes a source address bit pattern and a destination address bit pattern that are ~~each~~ processed by a task processor in accordance with a data tree. ~~The data tree includes multiple nodes linked by branches wherein an instruction that is associated with each node within the data tree is utilized for determining which branch is to be taken in accordance with the source address bit pattern or the destination address bit pattern.~~ A first bank of registers is utilized to load an instruction to be executed by ~~said~~ the task processor at ~~each~~ nodes of the data

tree in accordance with the source address bit pattern. A second bank of registers is utilized for loading an instruction to be executed by the task processor at ~~each~~ nodes of the data tree in accordance with the destination address bit pattern. A task scheduler enables the first bank of registers to transfer an instruction loaded therein for processing by the task processor only during even time cycles and for enabling the second bank of registers to transfer an instruction loaded therein for processing by the task processor only during odd time cycles.